R22 Regulation *Subject code:4E3FB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, June 2026

COMPUTER ORGANIZATION AND ARCHITECTURE

(IT)

Maximum Marks: 60 Date:20.06.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	What is meant by clock cycle time	1M	1	Remember
b)	Name the addressing mode used in auto increment / decrement	1M	1	Remember
c)	Which register holds the address of the next instruction	1M	2	Remember
d)	What is hardwired control unit	1M	2	Remember
e)	Name three types of data hazards	1M	3	Remember
f)	What is branch delay or branch penalty	1M	3	Remember
g)	What is flash memory	1M	4	Remember
h)	Where L1 cache is located	1M	4	Remember
i)	Expand SATA	1M	5	Remember
j)	What is interrupt vector table	1M	5	Remember

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	a) Explain the basic operational concepts using register transfer notation. b) Explain instruction sequencing with a flowchart.	5M 5M	1	Understand
	OR			
3	a) List and explain any six addressing modes with an example instruction. b) Explain Booth's algorithm for multiplication of signed numbers.	5M 5M	1	Understand
4	a) Explain in detail the data path for a single cycle processor. b) Explain the major hardware components of processing unit.	5M 5M	2	Understand
	OR			
5	a) Explain the generation of control signals in a CPU. b) Explain the characteristics of CISC style processors.	5M 5M	2	Understand
6	a) Explain how the memory delay affects the pipeline performance. b) Explain the challenges of pipelining in CISC processors.	5M 5M	3	Understand

	OR			
7	a) Classify the types of pipeline hazards with suitable example. b) Explain the performance metrics of a pipeline.	5M 5M	3	Analyze
8	a) Explain the different levels of cache memory (L1, L2, L3) b) Differentiate between. i. Static RAM vs Dynamic RAM ii. PROM vs EEPROM	5M 5M	4	Understand
	OR			
9	a) Explain the memory hierarchy in a computer system with a diagram. b) Explain the concept of virtual memory.	5M 5M	4	Understand
10	a) Compare the centralized and distributed bus arbitration. b) Explain the role of DMA in I/O organization.	5M 5M	5	Analyze
	OR			
11	a) Explain the advantages and disadvantages of program controlled I/O. b) Explain the three types of bus operations with timing diagrams.	5M 5M	5	Understand